

**Notice of Allowability**

Application No.

09/905,394

Examiner

John Pezzlo

Applicant(s)

ORNES ET AL.

Art Unit

2662

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--**

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to amendment filed 27 June 2005.
2. ☒ The allowed claim(s) is/are 1-11, 13-41 (renumbered 1-40 respectively).
3. ☒ The drawings filed on 13 July 2001 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) ☐ All    b) ☐ Some\*    c) ☐ None    of the:
  1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.


Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
  6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
    - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date \_\_\_\_\_.
    - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date \_\_\_\_\_
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date \_\_\_\_\_
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other \_\_\_\_\_

  
**JOHN PEZZLO**  
**PRIMARY EXAMINE**

## **DETAILED ACTION**

### ***Allowable Subject Matter***

Claims 1-11 and 13-41 are allowable over the prior art of record.

### ***Reasons for Allowance***

The following is an examiner's statement of reasons for allowance: Applicants have claimed the following uniquely distinct features in the instant invention which are not found in the prior art, either singularly or in combination:

1. Regarding claim 1 - An apparatus for reordering sequence information units comprising:  
(a) a double-back shifter having plural storage devices, the shifter being for receiving and simultaneously storing a plurality of sequence indicated information units in corresponding ones of its storage devices, where the received units can be initially organized logically and upon receipt in an initial sequential order other than a proper order defined by respective sequence indicators received with and included in the received information units, and indicated (b) at least a first test-and-reshuffle circuit coupled to first and second unit storage devices of said double-back shifter for testing the respective sequence indicators of valid information units, if any, stored in the first and second storage devices for proper relative order, and for reshuffling at least the relative logical order of the tested units within the double-back shifter if said testing shows the tested information units to be out of proper relative sequential order, said testing and

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reshuffling being repeatable for further information units that next shift into at least one of the first and second unit storage devices so that after being reshuffled, received but out of order information units can emerge in proper relative sequence when finally shifted out of said double-back shifter.

2. Regarding claim 18 - A method for reordering sequence indicated information units into proper sequence, comprising: (a) storing sequence indicated information units in a double-back shifter, (b) while the information units remain within the double-back shifter, repetitively comparing, reordering and shifting the sequence indicated information units within the double-back shifter so as to cause the information units to be in proper indicated sequence when shifted out of said double-back shifter.

3. Regarding claim 28 - A data reordering mechanism comprising: (a) a plurality of data storage units each for storing at least a corresponding, proper sequence indicator of a correspondingly received one of plural data payloads that were received in a given time period, but not necessarily received during the given time period in an order defined by their respective, proper sequence indicators, the plurality of data storage units defining part of a shifter through which the stored sequence indicators can be serially shifted, and (b) a plurality of test-and-reshuffle circuits each coupled at least to a corresponding two different data storage units within the shifter and each operative to cross-test valid sequence indicators respectively stored in the corresponding at least two data storage units against one another, said cross-testing including testing the relative logical sequence indicated by the respectively stored sequence indicators against the relative physical storage sequence that the tested sequence indicators have within the shifter to thereby determine if the relative physical storage sequence properly comports with the

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indicated, relative logical sequence of the cross-tested valid sequence indicators, (b.1) where upon determining that an improper relative physical storage sequence is present between two or more of its correspondingly cross-tested sequence indicators, each test-and-reshuffle circuit reshuffles the relative physical storage sequence within the shifter of its tested and improperly located sequence indicators, and reshuffles the relative physical storage sequence within the shifter of payload data and/or other payload related data stored in association with the improperly located sequence indicators so as to bring the relative physical storage sequence of the improperly located sequence indicators and their associated payload data or payload related data into better compliance with the relative logical sequence indicated by the respectively stored and cross-tested sequence indicators.

4. Regarding claim 35 - A data reordering method comprising: (a) storing in a plurality of data storage units, at least a plurality of corresponding, proper sequence indicators of correspondingly received ones of plural data payloads that were received in a given time period, but not necessarily received during the given time period in an order defined by their respective, proper sequence indicators, the plurality of data storage units defining part of a shifter through which the stored sequence indicators can be serially shifted, and (b) using a plurality of test-and-reshuffle circuits, each coupled to a corresponding at least two different data storage units within the shifter, for cross-testing valid sequence indicators respectively stored in the corresponding at least two data storage units against one another, said cross-testing including testing the relative logical sequence indicated by the respectively stored sequence indicators against the relative physical storage sequence that the tested sequence indicators have within the shifter to determine if the relative physical storage sequence properly comports with the indicated, relative logical

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sequence of the cross-tested valid sequence indicators, (b.1) upon determining that an improper relative physical storage sequence is present between two or more of its correspondingly cross-tested sequence indicators, reshuffling the relative physical storage sequence within the shifter of the tested and improperly located sequence indicators so as to bring the relative physical storage sequence of the improperly located sequence indicators into better compliance with the relative logical sequence indicated by the respectively stored sequence indicators.

The closest prior art, either singularly or in combination, fail to anticipate or render the above limitations obvious.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

### ***Conclusion***

Claims 1-11 and 13-41 being allowable, **Prosecution On The Merits Is Closed** in this application.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. Gatherer (US 6,421,796 B1) discloses an efficient memory addressing convolutional interleaving.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Pezzlo whose telephone number is (571) 272-3090. The examiner can normally be reached on Monday to Friday from 8:30 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou, can be reached on (571) 272-3088. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2600.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C.

or faxed to:

(571) 273-8300

For informal or draft communications, please label "PROPOSED" or "DRAFT"

Hand delivered responses should be brought to:

Jefferson Building


2A15

500 Dulany Street

Alexandria, VA, 22313.

John Pezzlo

11 August 2005

  
**JOHN PEZZLO**  
**PRIMARY EXAMINER**